● General Description

The CH50P06N combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

- ■ Advance high cell density Trench technology
- ■Low $R_{DS(ON)}$ to minimize conductive loss
- ■Low Gate Charge for fast switching
- ■Low Thermal resistance

●Application

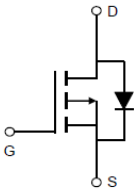
- ■SMPS 2nd Synchronous Rectifier
- ■POL application
- ■BLDC Motor driver

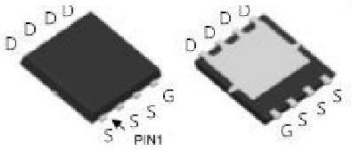
● Product Summary

V_{DS} =-60V

$R_{DS(ON)}$ =-23mΩ

I_D =-40A





DFN5 x 6

●Ordering Information:

Part NO.	CH50P06N
Marking	CH50P06N
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

●Absolute Maximum Ratings (T_C =25℃)

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}$TC=25℃	-40	A
	$I_{D@}$TC=75℃	27	A
	$I_{D@}$TC=100℃	22	A
Pulsed Drain Current ①	I_{DM}	-80	A
Total Power Dissipation	P_D@TC=25℃	55	W
Total Power Dissipation	P_D@TA=25℃	2.5	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃
Single Pulse Avalanche Energy@L=0.1mH	E_{AS}	100	mJ
Avalanche Current@L=0.1mH	I_{AS}	30	A
ESD Level (HBM)		Class 2	

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	2.1	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	50	° C/W
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =-250uA	-60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =-250uA	-1.2		-2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-60V, V_{GS} =0V			-1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-15A		23	32	mΩ
		V_{GS}=-4.5V, I_D=-10A		29	38	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-10V, I_D=-10A		20		s

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	Ciss	f = 1MHz	-	3300	-	pF
Output capacitance	Coss		-	148	-	
Reverse transfer capacitance	Crss		-	96	-	

●Gate Charge characteristics(T_a = 25℃)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Qg	V_{DD} =-25V	-	46	-	nC
Gate - Source charge	Qgs	I_D =-10A	-	6.3	-	
Gate - Drain charge	Qgd	V_{GS} =-10V	-	8.6	-	

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

Fig.1 Gate-Charge Characteristics

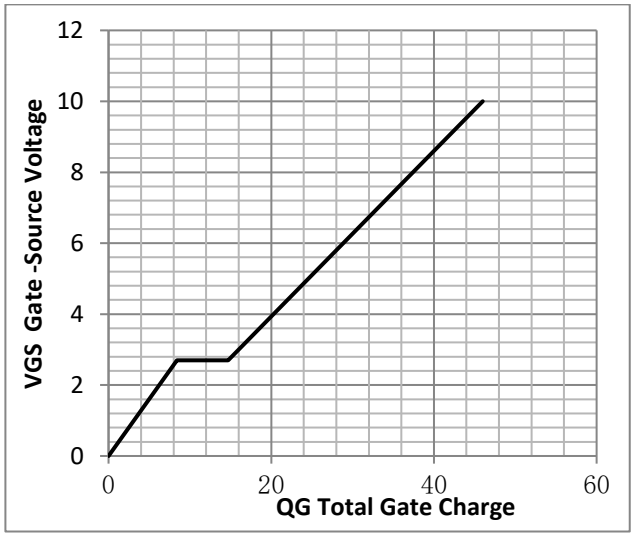


Fig.2 Capacitance Characteristics

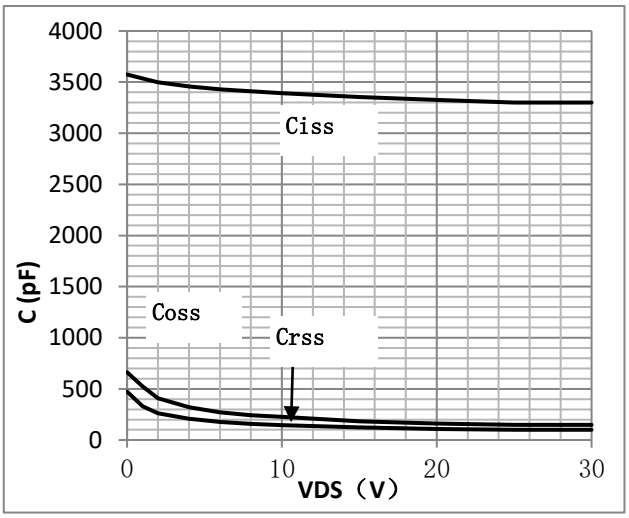


Fig.3 Power Dissipation

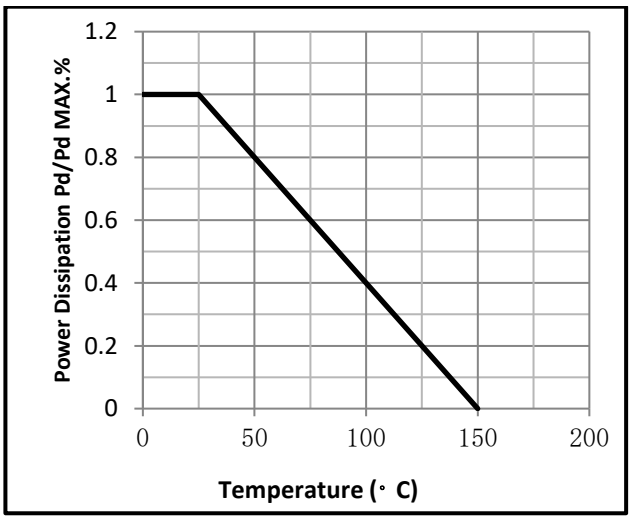


Fig.4 Typical output Characteristics

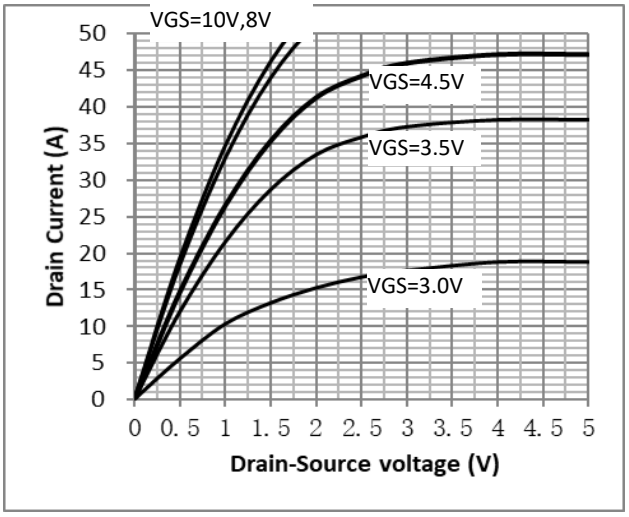


Fig.5 Threshold Voltage V.S Junction Temperature

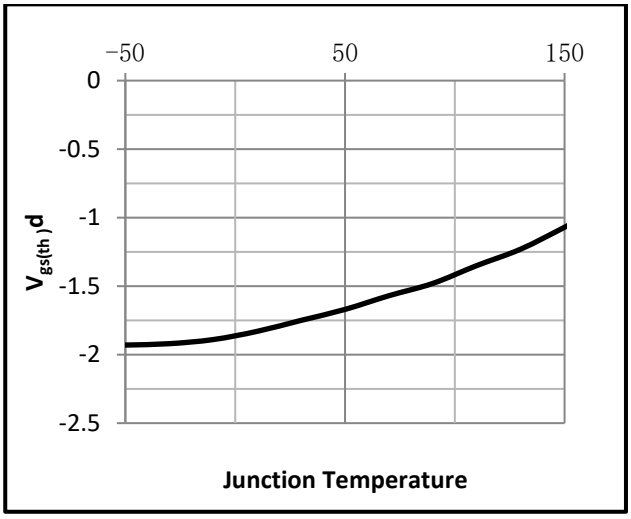


Fig.6 Resistance V.S Drain Current

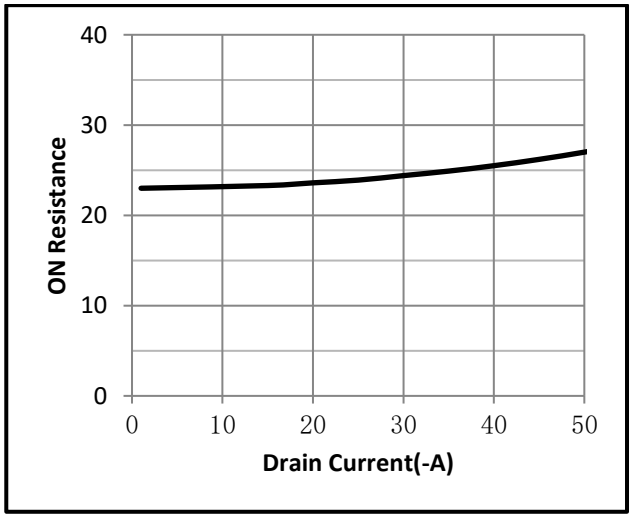


Fig.7 On-Resistance VS Gate Source Voltage

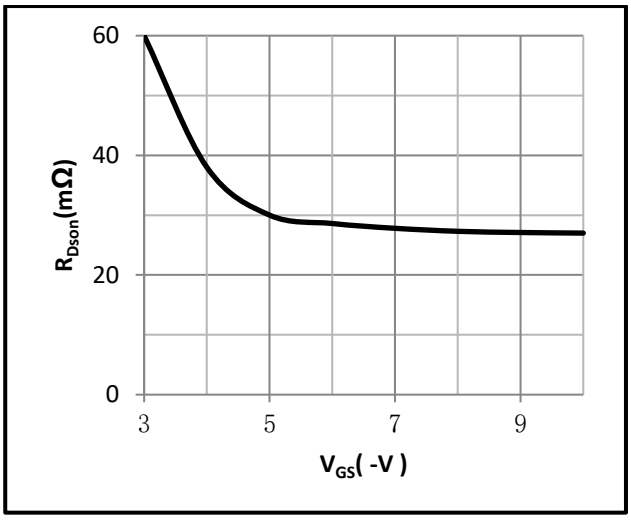


Fig.8 On-Resistance V.S Junction Temperature

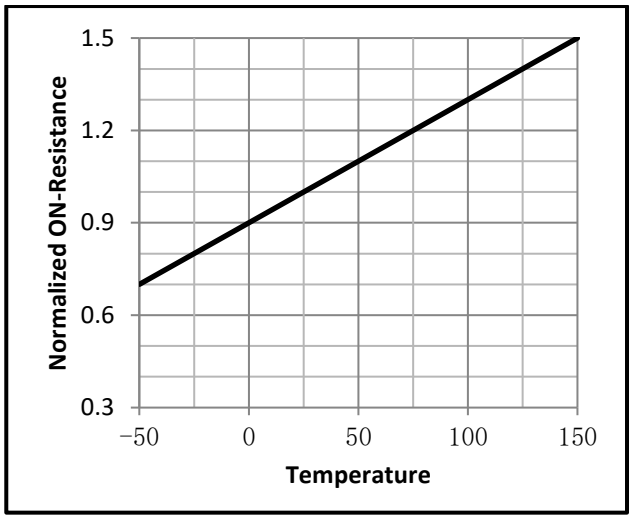
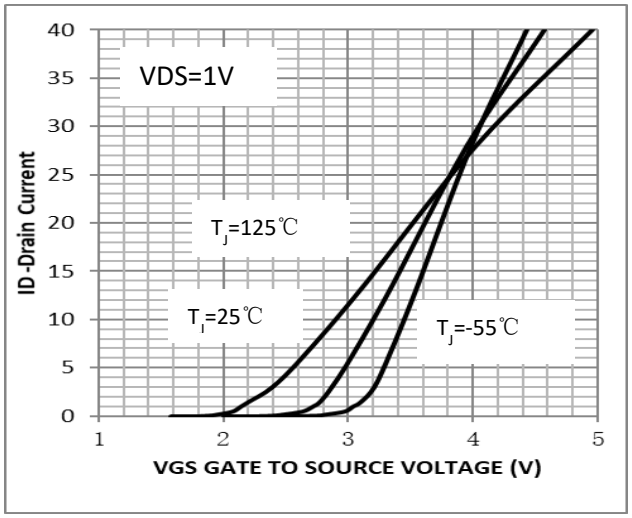


Fig.9 Transfer Characteristics



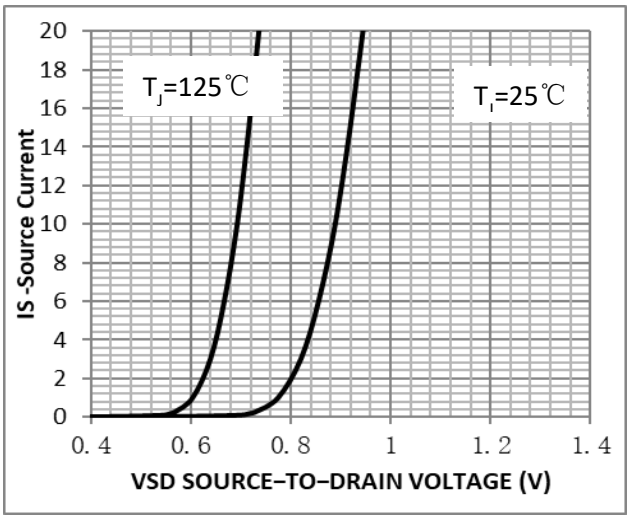


Fig.9 SOA Maximum Safe Operating Area

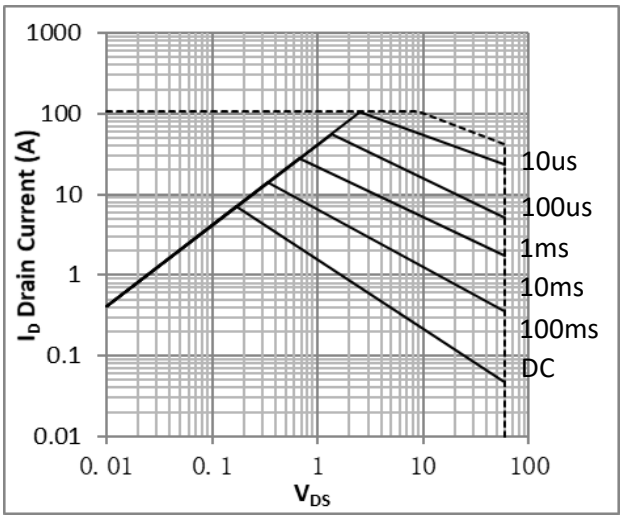


Fig.10 ID-Junction Temperature

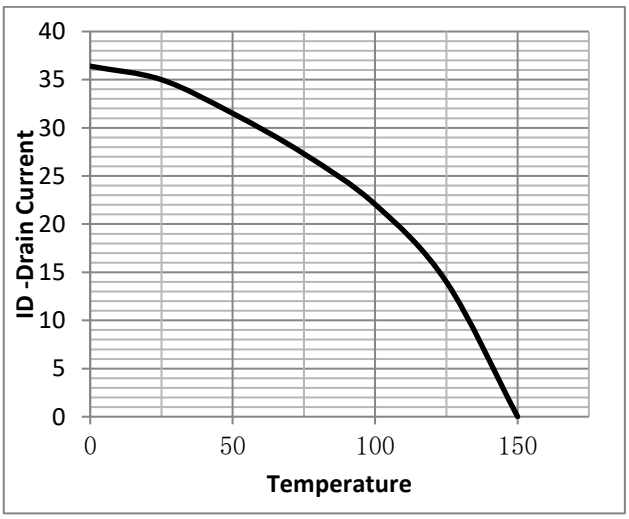


Fig.10 Switching Time Measurement Circuit

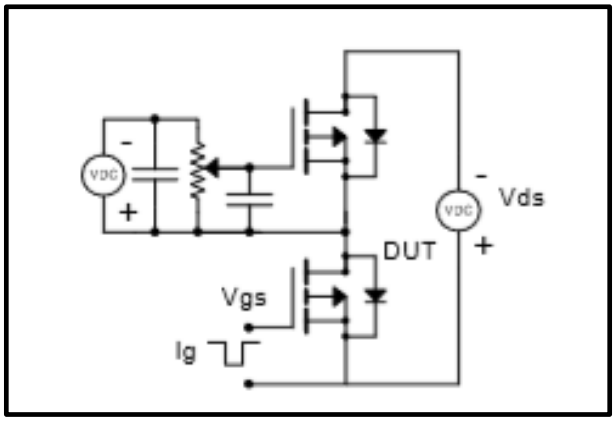


Fig.11 Gate Charge Waveform

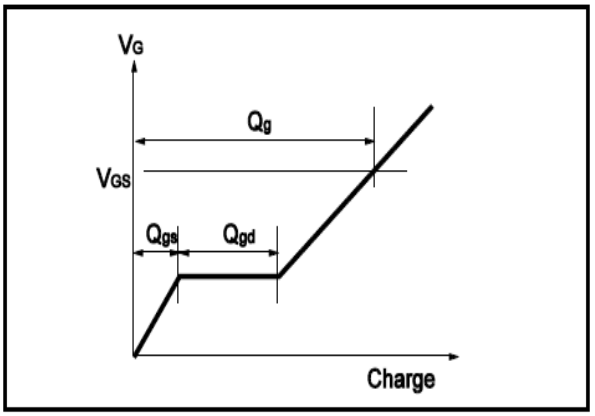


Fig.12 Switching Time Measurement Circuit

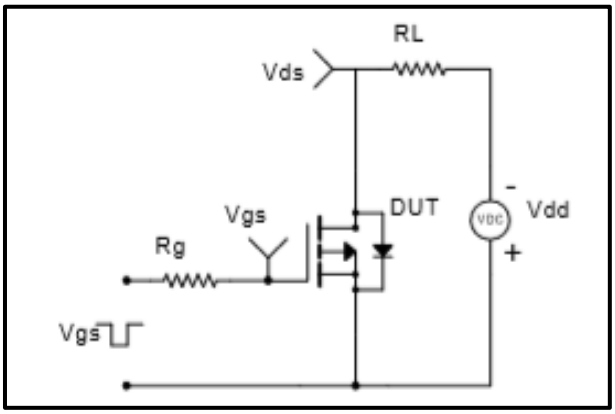
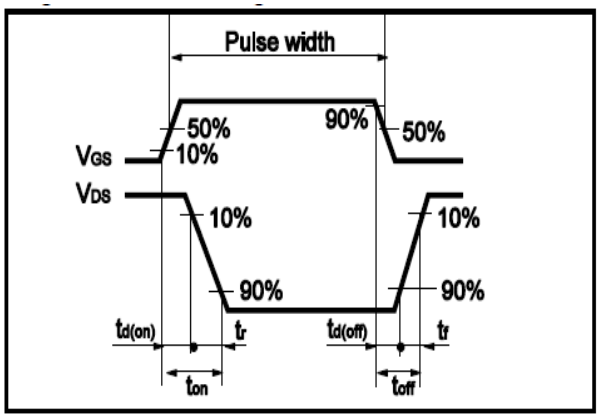
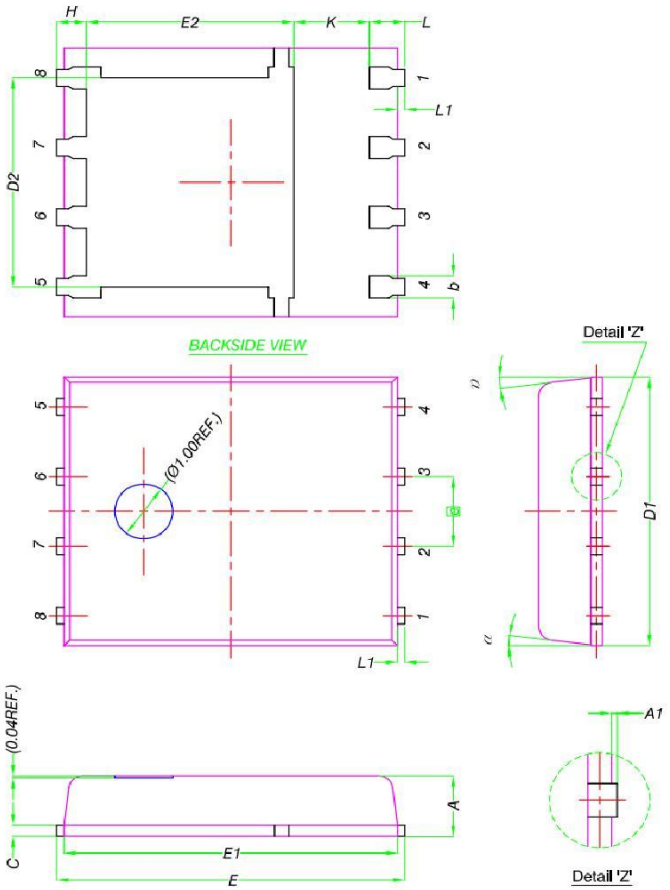


Fig.13 Gate Charge Waveform



•Dimensions DFN5×6



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°